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Electro-thermal simulation: a new Subsystem in Mentor Graphics IC Design Flow

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***Abstract*-New electro-thermal simulation subsystem was introduced into Mentor Graphics IC Design flow. The subsystem incorporates IC thermal simulation tool "Overheat", dispatcher "ETh SimCoupler" as the simulation manager and layout converter "ETh Model Generator". Application example of power voltage regulator IC simulation is described. A good agreement between simulated and IR-camera measured temperature pictures is achieved.**

Index Terms- **Electro-thermal simulation, IC, CAD.**

I. Introduction

Constant decreasing of IC element dimensions, ever increasing packing density of ICs, combining of digital and analog blocks, integration of elements with low and high power consumption on the same chip lead to a number of complex problems connected with high working temperatures and mutual thermal influence of IC elements as a result of increasing power density.

Elements of semiconductor IC is known to be sensitive to temperature changes. For example, temperature rise of 1 ºC leads to 2 mV fall in forward biased p-n junction. And in the case of temperature rise of 10 ºC the current of reverse biased p-n junction is doubled.

Power dissipation of some IC and VLSI types may be 10..100 W, which leads to significant temperature rise of the chip. For industrial and domestic smart power ICs the area of power BJT, DMOST, IGBT output devices takes 30-70% of the chip size. For instance, Intel Xeon series 7100, produced by deep submicron 65 nm technology, dissipates 150 Watt. Its case and junction temperatures are 70 ºC and 90 ºC. It is known that temperature of Si ICs should not be higher 120-150 ºC to operate properly.

For analog and mixed type ICs the temperature gradients on the chip are as much critical as the temperatures of components. For example, temperature difference of transistors, connected to input branches of operational amplifiers, comparators, high precision DAC/ADCs normally should not be more than 0.1-0.3 ºC.

Therefore presence of "hot spots" (as places of local overheat) leads to significant changes of electrical parameters of element or element groups, which results in chip performance degradation. High temperature impacts not only electrical parameters of ICs, but they force undesirable physical-chemical processes in semiconductor material and IC construction as well. These may lead finally to the fault of IC.

Factors mentioned above make IC developers to hardly constrain working temperatures of elements, introduce thermal protection circuits and improve cooling.

As conclusion, electro-thermal simulation is one of the most important stages of modern ICs and VLSIs design. This simulation let to choose optimal electrical and thermal modes for different elements, develop IC layout and construct, resulting in: 1) minimal junction temperatures of devices; 2) minimal mutual influence of elements through the bulk; 3) better conditions of thermal transfer to case, heat sink and environment; 4) minimal thermal gradients excluding thermal strain of materials.

There are two major approaches to doing electrothermal simulation.

In the first approach (called – **relaxation method**) two independent simulators, one thermal simulator, solving numerically heat conduction problem, and one electrical circuit simulator (SPICE or its modifications) are used in iterative loop to deliver the solution of the given electrothermal problem [1], [2]. The advantages are: the high accuracy and visualization; the on-chip or on-board steady-state 2D or 3D temperature profiles directly identify hot spots and „poor" components; the ability to move different

components (heat sources) on the chip/board layout to correct the temperature map. The drawbacks are: in case of very strongly couled electrothermal problem, the solution cannot achieve convergence; the approach is computational time consuming and limited by the very large number of mesh points due to numerical solution methods.

In the second approach (called – **direct method**) the thermal subsystem is represented by an electrical model network and an electrical solver (SPICE, SPECTRE, ELDO) performs simultaneously co-simulation of both electrical and thermal subsystems [3]. The advantages are: capability to achive a fast thermal solution even in case of strongly coupled electrothermal problem; more simpler preparation and implementation of design task. The drawbacks are: less accurate thermal solution in the form of the set of average temperatures of components; poor ability to change the placement of components to improve the thermal condition.

Earlier SISSI electro-thermal simulation software package was reported to be included in Cadence IC Design Flow [4], [5]. Mentor Graphics lacks thermal modeling packages in its IC Design Flow, so its capabilities are limited, particularly in development of power analog and mixed type ICs for industrial control, automotive electronics, power regulators and others.

This paper describes fully automated subsystem for electro-thermal simulation of ICs introduced into Mentor Graphics IC Design Flow (IC Station).

II. Electro-Thermal Simulation Subsystem

Relaxation method using simulator coupling approach was chosen to introduce electro-thermal simulation into Mentor Graphics IC Station. Electrical simulation is carried out by Eldo – Mentor Graphics SPICE analog. Thermal simulation is carried out by quasi-3d computational IC thermal simulator named Overheat [6]. These simulators are coupled through number of sequential iterations. First element temperatures approximation is used in Eldo to compute IC electrical behavior and powers dissipated by the elements. Then these powers are used by Overheat to compute new temperatures of elements, which differ from firstly approximated. New temperatures are used by Eldo again to compute powers for Overheat etc. These iterations are repeated until thermal and electrical behaviors become stable from iteration to iteration.

Developed flow chart of electro-thermal simulation is shown in fig. 1. New blocks introduced in Mentor Graphics IC Station and their links are shown in bold lines.

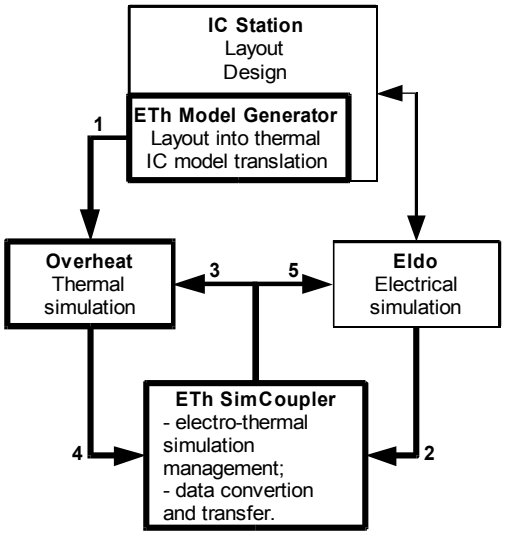

Fig. 1. Flow chart of electro-thermal simulation in Mentor Graphics IC Station.

"**Overheat**" – quasi-3d computational thermal simulator for monolithic ICs. The chip, fixed in the package is represented as multi-layer structure (fig. 2); its layers have different heat characteristics. The heat sources are circuit elements (transistors, resistors, etc.), the heat dissipates from package surface by convection into environment and through lead-out wire.

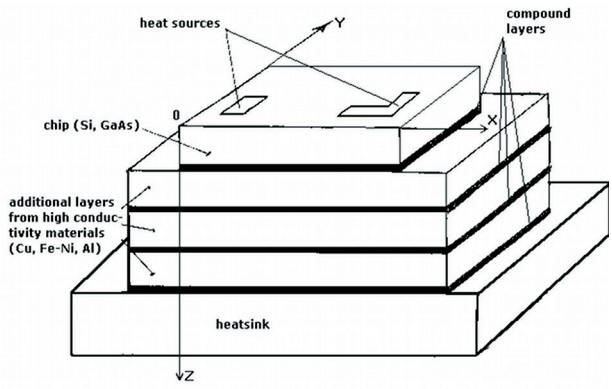

Fig. 2. Model of multi-layer IC structure used in Overheat.

The mathematical model is the three-dimensional heat conduction equation:

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}=0 \qquad (1)$$

with the following boundary conditions:

a) on the boundary between chip and air:

$$\lambda_1 \frac{\partial T}{\partial z}\bigg|_{z=0} = -P(x,y)+\alpha(T-T_{env}) \quad , \qquad (2)$$

$$P(x,y)=\begin{cases} P_{el}/S_{el}, (x,y)\in S_{el}, \\ 0, (x,y)\notin S_{el}, \end{cases}$$

b) on the boundaries of different layers:

$$\lambda_{-i} \frac{\partial T}{\partial z}\bigg|_{z=z_i-0} = \lambda_{i+1} \frac{\partial T}{\partial z}\bigg|_{z=z_i+0} \quad , \qquad (3)$$

$$T(x,y,z_i-0)=T(x,y,z_i+0) \qquad (4)$$

c) on the bottom of the package there are two variants:

1) the heat conduction of package is large (metallic package) its temperature is constant, but it is not equal to environmental temperature, then the bottom of parallelepiped is the bound solder – package, or compound – package, and the boundary condition:

$$T(x,y,z_n)=T_{pack}=const \qquad (5)$$

2) the package is not isothermal through the little heat conduction (plastic package), then the bottom of parallelepiped is the bound air – package and there is the convective heat exchange on it:

$$\lambda_{-n} \frac{\partial T}{\partial z}\bigg|_{z=z_n} = \alpha(T(x,y,z_n)-T_{env}) \qquad (6)$$

d) there is no heat exchange on the lateral surfaces of the chip:

$$\frac{\partial T}{\partial x}\bigg|_{x=0} = \frac{\partial T}{\partial x}\bigg|_{x=x_C} = \frac{\partial T}{\partial y}\bigg|_{y=0} = \frac{\partial T}{\partial y}\bigg|_{y=y_C} = 0 \qquad (7)$$

In equations (1) – (7) the following notations are used: T – absolute temperature (K), P_{el} – power of element (W), S_{el} – area of element (mm^2), λ_i – coefficients of thermal conductivity of layers (W/mm·K), T_{pack} – temperature of package (K), T_{env} – the environmental temperature (K), α – coefficient of convective heat exchange (W/mm^2·K), x_C , y_C – the chip sizes on layout plane (mm), z_i – the layer co-ordinates.

Thermal conductivity of silicon depends on temperature:

$$\lambda_{Si}=311.0/T^{4/3} \quad , \quad \text{W/mm·K}, \qquad (8)$$

For solving of the three-dimensional heat conduction equation (1) with the boundary conditions (2) – (7) we use the separation of variables method with the discrete Fourier transformation and fast Fourier transformation algorithms (FFT) [7]. The solution of equation (1) has the form:

$$T_{i,j}=F^{-1}(F(P_{i,j})\cdot\Theta_{k,l,1}), \quad i=0,\ldots,M_x \ , \ j=0,\ldots,M_y \ , \qquad (9)$$

where: $T_{i,j}$ and $P_{i,j}$ – the temperature of top of the chip and power density in the difference network nodes respectively; $F(\cdot)$, $F^{-1}(\cdot)$ – right and inverse discrete Fourier transformations, respectively:

$$\tilde{f}_{k,l}=F(f_{i,j})= \frac{2}{\sqrt{M_x M_y}} \sum_{i=0}^{M_x} \sum_{j=0}^{M_y} f_{i,j} \cos\left(\frac{k\pi i}{M_x}\right) \cos\left(\frac{l\pi j}{M_y}\right) ,$$

$$f_{i,j}=F^{-1}(\tilde{f}_{k,l})= \frac{2}{\sqrt{M_x M_y}} \sum_{k=0}^{M_x} \sum_{l=0}^{M_y} \tilde{f}_{k,l} \cos\left(\frac{k\pi i}{M_x}\right) \cos\left(\frac{l\pi j}{M_y}\right) ;$$

factors $\Theta_{k,l,1}$, $k=0,\ldots,M_x$, $l=0,\ldots,M_y$ are determined from the boundary conditions.

Overheat input data consist of four types of parameters:

1. parameters, describing IC package: number and type of each construct layer, its sizes, physical and thermal properties of the material;
2. parameters describing IC layout: number and type of each elements; its configuration sizes, thermal conductivity;
3. powers of IC elements;
4. parameters directing the simulation process: $M_x \times M_y$ grid sizes, accuracy of solutions.

Output data:

1. $M_x \times M_y$ matrix of temperatures in (i,j) grid points;
2. multi-color temperature map of IC chip;
3. average and maximal temperatures of elements.

Execution time rises as $M * \ln(M)$, where M – grid size in one dimension. Overheat was developed for GNU/Linux operating system for including into developed electro-thermal simulation subsystem.

ETh SimCoupler – dispatcher program is developed to manage thermal and electrical simulators and their

interaction. ETh SimCoupler converts data transferred between simulators (Overheat and Eldo) and launches them, when appropriate. The program runs under GNU/Linux operating system.

ETh Model Generator – converter for changing layout data format from IC Station into Overheat input file format. ETh Model Generator is developed as additional component to layout editor IC Station.

The flow chart of electro-thermal simulation is shown in fig. 1. Simulation begins with thermal model generation (arrow #1 in fig. 1) made by ETh Model Generator. It requires layout to be fully developed in IC Station and corresponding electrical netlist to be successfully simulated in Eldo. On the second stage ETh SimCoupler is launched to manage iteration simulation and transfer data between Overheat and Eldo. ETh SimCoupler runs Eldo and reveals information about powers from this simulation (arrow #2 in fig. 1); writes these information into Overheat input file (arrow #3 in fig. 1); runs thermal simulation through Overheat and reveals temperature information (arrow #4 in fig. 1); forms new Eldo input file using gained temperatures (arrow #5 in fig. 1). Simulation is looped this way (stages from 2 to 5 in fig. 1) until values of dissipated powers of elements on two consequential iterations differ less then ΔP parameter.

III. Application Example

The effectiveness of developed electro-thermal subsystem fig. 1 is demonstrated in the example of power voltage regulator IC K142EN9 (see fig. 1). Input voltage is 40 V, output voltage 27 V, output current 270 mA, total power about 11 W.

The IC chip layout with sizes 2 mm X 2 mm (see fig. 4) was covered in Overheat by the 513x513 grid for numerical quasi-3d solution of heat transfer equation (1).

IBM PC compatible computer (RAM – 512 Mb, CPU frequency – 1.8 GHz) with GNU/Linux version 2.4.18 operating system was used. Simulation finished in 3 iterations and took 14 seconds. Power accuracy parameter (ΔP) was set to 10 mW.

In fig. 4 isothermal lines on the IC chip surface are shown.

IV. IR Thermography of IC chip

IR camera A40 of FLIR Systems with 18 μm macrolens was used to measure IC chip thermal map and temperatures of elements. Camera thermal sensitivity is 80 mK when temperature is 25 ºC, resolution is 320x240 pixels, tolerance +/- 2 ºC. IC chip thermal map is shown in fig. 5. Comparing simulated and measured thermal maps shown in fig. 4 and 5, one can see sufficient accuracy. The differences in temperatures of IC elements are 2-5 ºC (see Table 1).

TABLE 1
Simulated and measured temperatures comparison

Dot	Temperature		Difference
	Measured	Simulated	
A	355.2 K	353.5 K	1.7 K
B	353.0 K	353.0 K	0.0 K
C	347.2 K	350.4 K	3.2 K
D	343.4 K	339.5 K	3.9 K
E	341.1 K	339.9 K	1.2 K

V. Conclusions

Fully automated electro-thermal simulation subsystem is introduced into Mentor Graphics IC Station Design System.

Efficiency of new electro-thermal subsystem were demonstrated by the examples of different types of power analogue and mixed A/D ICs produced by different semiconductor technologies [8].

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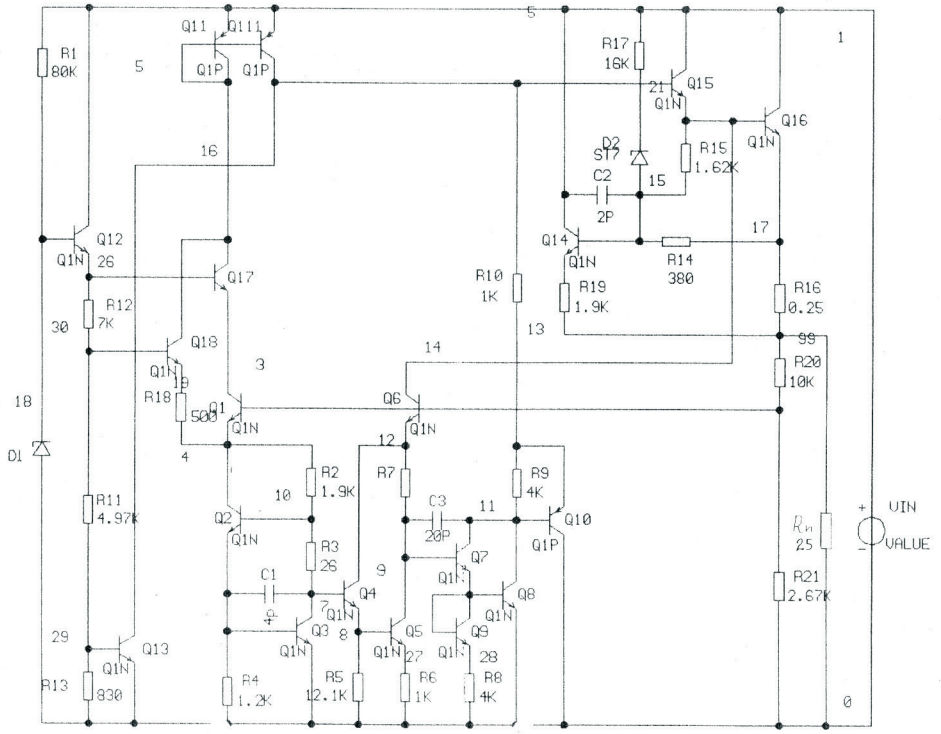

Fig. 3. Power voltage regulator IC schematic (K142EN9).

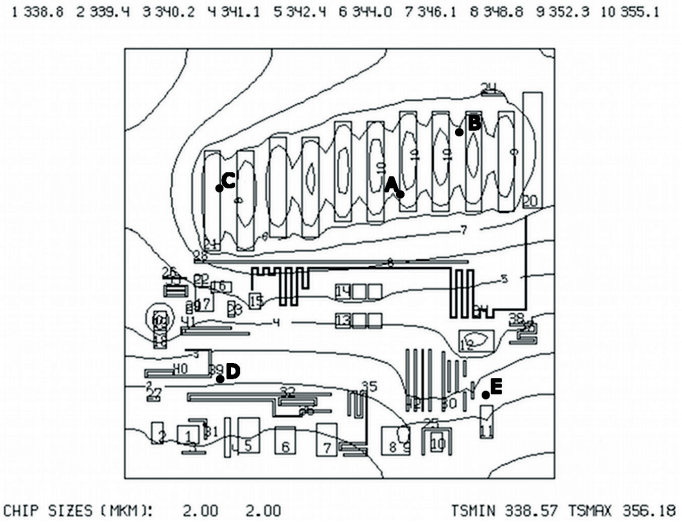

Fig. 4. Simulated thermal map of K142EN9 IC.

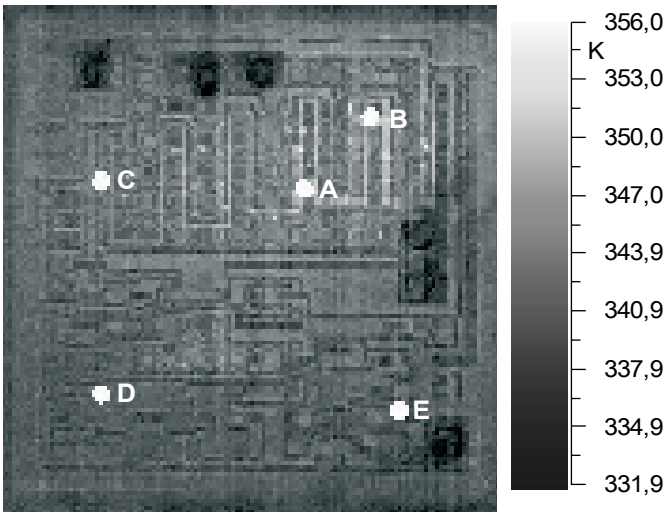

Fig. 5. Thermal distribution on top of K142EN9 IC, measured using IR thermography.

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